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(71) Applicant: **Samsung Electronics Co., Ltd.**
Suwon-si, Gyeonggi-do (KR)

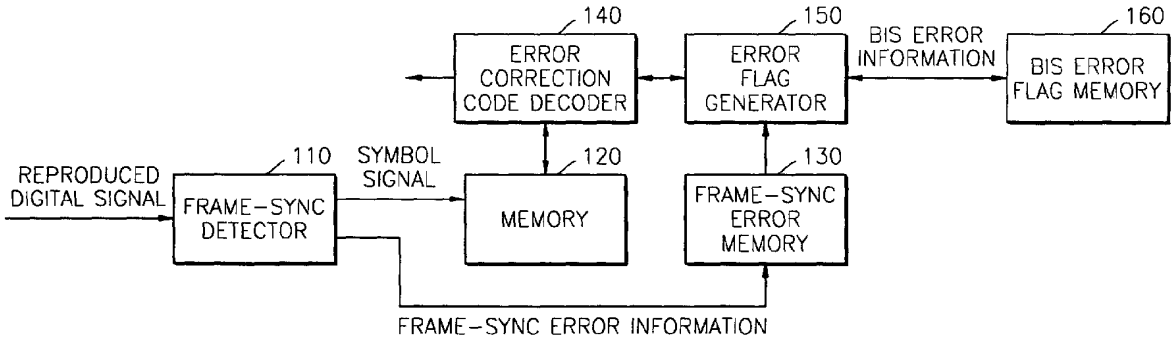
(72) Inventors:
- **Hwang, Sung-hee**
  Gangnam-gu Seoul (KR)
- **Park, Hyun-jung**
  Gwonseon-gu, Suwon-si Gyeonggi-do (KR)
- **Kim, Joo-seon**
  Jungwon-gu, Seongnam-si Gyeonggi-do (KR)
- **Ryu, Sang-hyun**
  Yeongtong-gu, Suwon-si Gyeonggi-do (KR)

(74) Representative: **Robinson, Ian Michael et al**
Appleyard Lees,
15 Clare Road
Halifax HX1 2HY (GB)

(54) Apparatus and method generating error flags for errors and erasures decoding

(57) An error flag generation apparatus and method for error correction, wherein the apparatus includes: a frame-sync error memory (130) which stores frame-sync error information for each data block; a BIS (Burst Indicator Subcode) error flag memory (160) which stores a BIS error flag for each data block; and an error flag generator (150), which generates an error flag indicating error existence/absence for ECC (Error-Correction Coding) data with reference to the frame-sync error information stored in the frame-sync error memory (130) and the BIS error flag stored in the BIS error flag memory (160). The error correction code decoder (140) receives an error flag generated by the error flag generator (150) and performs erasure correction for the symbol signal stored in the memory (120) for each data block. The error flag generation apparatus and method for error correction can be easily implemented with improved error-correction performance and be advantageous in cost.

FIG. 3



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Description

[0001] The present invention relates to an apparatus and method generating an error flag for error correction.

[0002] To store information in an optical recording medium such as CD or DVD, error-correction coding (ECC) is performed in which parity data is added to user data to generate a codeword and the codeword is processed according to a predetermined method. If the user data is 30 bytes, the parity data is 30 bytes, and accordingly one codeword is 60 bytes, error correction is possible although errors are generated in maximal 15 bytes of one codeword when decoding is performed. However, if an error flag indicating the location of data including an error in the codeword is provided, error correction is possible although errors are generated in maximal 30 bytes of the codeword.

[0003] Such a technique that improves error correction performance using an error flag is called erasure correction. The erasure correction has higher error correction efficiency where a burst error is generated rather than a random error.

[0004] U.S. Patent No. 6,367,049 discloses an error correction format consisting of a plurality of ECC (Error Correction Code) columns and a plurality of BIS (Burst Indicator Subcode) columns. BIS is information that is inserted when decoding is performed, in order to indicate the generation of a burst error. A reliability of a decoded BIS is higher than that of ECC.

[0005] Figure 1 is a view showing a data block with an error correction format disclosed in the above-described U.S. Patent No. 6,367,049.

[0006] According to the error correction format, in one data block, frame synchronization (frame-sync) data is included in the heading of the data block, and subsequently 38 ECC columns and one BIS column are located alternately. One data block has 496 frames. Data constructing the data block is interleaved according to a predetermined method. The detailed descriptions related to the error correction format and interleaving are disclosed in the above-described U.S. Patent Application No. 6,367,049.

[0007] Figure 2 shows a detailed structure of one frame forming part of the data block of Figure 1.

[0008] Referring to Figure 2, in one frame, frame-sync data is included in the heading of the frame and subsequently 38-byte ECC and one-byte BIS are located alternately.

[0009] However, an error correction system according to the error correction format shown in Figures 1 and 2 has problems in that an interleaving process is complex, accordingly the generation of an error flag for erasure correction is not easy, and a hardware structure is complicated.

[0010] The present invention provides an apparatus and method generating an error flag for error correction, having improved performance and being advantageous in cost.

[0011] According to the present invention there is provided an apparatus and method as set forth in the appended claims. Preferred features of the invention will be apparent from the dependent claims, and the description which follows.

[0012] According to an aspect of the present invention, there is provided an apparatus generating an error flag, the apparatus including: a frame-sync error memory which stores frame-sync error information for each data block; a BIS (Burst Indicator Subcode) error flag memory which stores a BIS error flag for each data block; and an error flag generator, which generates an error flag indicating error existence/absence for ECC (Error-Correction Coding) data with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory.

[0013] According to another aspect of the present invention, there is provided an error flag generation method comprising: receiving a reproduced digital signal; generating frame-sync error information for each data block using the reproduced digital signal; storing the frame-sync error information in a frame-sync error memory for each data block; generating a BIS error flag of the data block for each data block; storing the BIS error flag of the data block in a BIS error flag memory for each data block; and generating an error flag indicating error existence/absence for ECC data with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory.

[0014] Additional aspects and/or advantages of the invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the invention.

[0015] For a better understanding of the invention, and to show how embodiments of the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings in which:

Figure 1 is a view showing a data block with an error correction format according to a conventional technique;

Figure 2 shows a detailed structure of one frame forming part of the data block of Figure 1;

Figure 3 is a block diagram of an apparatus for generating an error flag, according to an embodiment of the present invention;

Figures 4A-4C are timing charts describing the generation of a frame synchronization (frame-sync) error signal;

Figure 5 is a view showing a structure of a frame synchronization (frame-sync) error memory of Fig-

ure 3;

Figure 6 is a view showing a structure of a BIS (Burst Indicator Subcode) error flag memory of Figure 3; and

Figure 7 is a flowchart illustrating a method for generating an error flag, according to an embodiment of the present invention.

[0016] Reference will now be made in detail to the embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiments are described below to explain the present invention by referring to the figures.

[0017] Figure 3 is a block diagram of an apparatus generating an error flag, according to an embodiment of the present invention. Referring to Figure 3, the error flag generation apparatus includes a frame synchronization (frame-sync) detector 110, a memory 120, a frame synchronization (frame-sync) error memory 130, an error correction code decoder 140, an error flag generation unit 150, and a BIS (Burst Indicator Subcode) error flag memory 160.

[0018] The frame-sync detector 110 receives a reproduced digital signal, and outputs frame-sync error information indicating an error existence/absence for frame-sync data of frames forming a data block, to the frame-sync error memory 130. The frame-sync detector 110 also outputs a symbol signal for error correction to the memory 120. The digital signal input to the frame-sync detector 110 is a signal read from information stored in a disk (not shown) using an optical head (not shown), subjected to a highfrequency signal processing and equalizing, and reproduced.

[0019] Figures 4A- 4C are timing charts describing the generation of a frame-sync error signal by the frame-sync detector 110.

[0020] The frame-sync detector 110 generates a pseudo sync signal, shown in Figure 4B coinciding with a frame-sync signal existing in an original digital signal. The frame-sync detector 110 compares the generated pseudo sync signal with a frame-sync signal of the reproduced digital signal, shown in Figure 4C, and generates a frame-sync error signal, shown in Figure 4A.

[0021] The memory 120 receives and stores the symbol signal for error correction transmitted from the frame-sync detector 110. The memory 120 stores the symbol signals with the error correction code format as shown in Figures 1 and 2 for each data block.

[0022] The frame-sync error memory 130 receives and stores the frame-sync error information transmitted from the frame-sync detector 110.

[0023] Figure 5 is a view showing the structure of the frame-sync error memory 130. Referring to Figure 5, the frame-sync error memory 130 has first through N-th frame-sync error memories each having the size of 1 x 496 bits and being capable of storing information of 496 bits indicating an error existence/absence for each of the 496 sync data included in one data block. Accordingly, frame-sync error information for one data block is stored in a frame-sync error memory with the size of 1 x 496 bits. N frame-sync error memories each having the size of 1 x 496 bits are provided to store frame-sync error information of N data blocks, considering the timing between the generation of a BIS error flag by the error correction code decoder 140 and the storage of the BIS error flag by the BIS error flag memory 160. According to an embodiment of the present invention, N is three.

[0024] The error correction code decoder 140 performs error-correction for BIS of the data block stored in the memory 120. Then, the error-correction code decoder 140 outputs a BIS error flag as information indicating an error existence/absence for each symbol of BIS to the error flag generator 150. The error flag generator 150 outputs the BIS error flag to the BIS error flag memory 160.

[0025] Thereafter, the error correction code decoder 140 receives an error flag generated by the error flag generator 150 and performs erasure correction for the symbol signal stored in the memory 120 for each data block.

[0026] The error flag generator 150 generates an error flag for erasure correction using the frame-sync error information stored in the frame-sync error memory 130 and the BIS error flag stored in the BIS error flag memory 160, and outputs the error flag to the error correction code decoder 140.

[0027] Referring to Figure 2, the error flag generation operation of the error flag generator 150 will be described in detail. As shown in Figure 2, one data frame includes four ECC data, each being 38 bytes wherein each ECC data is located between frame-sync data and BIS data or between BIS data and BIS data.

[0028] If both frame-sync error information and a BIS error flag of the frame-sync data and the BIS data which are neighboring a corresponding 38-byte ECC data, or both BIS error flags of BIS data which are neighboring a corresponding 38-byte ECC data indicate error existence, the error flag generator 150 generates an error flag requiring erasure correction for the corresponding 38-byte ECC data, with reference to error information stored in the frame-sync error memory 130 and the BIS error flag memory 160.

[0029] The BIS error flag memory 160 receives the BIS error flag generated by the error correction decoder 140 via the error flag generator 150 and stores the received BIS error flag.

[0030] Figure 6 is a view showing the structure of the BIS error flag memory 160. Referring to Figure 6, one data block includes three BIS columns, with each BIS being 1 byte wherein each BIS column has 496 rows. Therefore, the BIS error flag memory 160 has first and M-th BIS error memories each being 1 x 496 bits and

being capable of storing information of 496 bits indicating an error existence/absence for each BIS data included in one data block. According to an embodiment of the prevent invention, M is three.

[0031] Hereinafter, an error flag generation method according to the present invention will be described in detail.

[0032] Figure 7 is a flowchart illustrating an error flag generation method according to an embodiment of the present invention.

[0033] The frame-sync detector 110 receives a reproduced digital signal for each data block (operation 210).

[0034] The frame-sync detector 110 generates frame-sync error information indicating an error existence/absence for the frame-sync data of each of the frames having a data block, and outputs the frame-sync error information to the frame-sync error memory 130 (operation 220). Also, the frame-sync detector 110 outputs a digital signal for error correction to the memory 120 for each data block.

[0035] The frame-sync error memory 130 receives the frame-sync error information corresponding to one data block from the frame-sync detector 110 and stores the received frame-sync error information (operation 230).

[0036] The frame-sync error memory 130 has first through N-th frame-sync error memories each being the size of 1 x 496 bits and being capable of storing information of 496 bits indicating an error existence/absence for the 496 sync data included in one data block. According to an embodiment of the present invention, N is three. Meanwhile, N frame-sync error memories each having the size of 1 x 496 bits are provided to store the frame-sync error information of three data blocks, considering the timing between the generation of the BIS error flag by the error correction code decoder 140 and the storage of the BIS error flag by the BIS error flag memory 160.

[0037] The error correction code decoder 140 performs error-correction for BIS of the data block stored in the memory 120 and generates a BIS error flag as information indicating error existence/absence for each symbol of BIS (operation 240).

[0038] The error correction code decoder 140 outputs the generated BIS error flag to the error flag generator 150. The error flag generator 150 outputs the BIS error flag to the BIS error flag memory 160 and the BIS error flag memory 160 stores the BIS error flag (operation 250). The BIS error flag memory 160 has first through M-th BIS error memories each being the size of 1 x 496 bits and being capable of storing information of 496 bits, in order to indicate an error existence/absence for each BIS data included in one data block. According to an embodiment of the present invention, M is three.

[0039] The error flag generator 150 generates an error flag for erasure correction using the frame-sync error information stored in the frame-sync error memory 130 and the BIS error flag stored in the BIS error flag memory 160 (operation 260).

[0040] The error flag generator 150 generates an error flag requiring erasure correction of corresponding 38-byte ECC data, with reference to error information stored in the frame-sync error memory 130 and the BIS error flag memory 160, if both frame-sync error information of frame-sync data and a BIS error flag of BIS data which are neighboring a corresponding 38-byte ECC data, or both BIS error flags of BIS data which are neighboring a corresponding 38-byte ECC data indicate error existence.

[0041] The error correction code decoder 140 receives the error flag generated by the error flag generator 150 and performs erasure correction of the symbol signal stored in the memory 120 for each data block (operation 270).

[0042] As described above, the error flag generation apparatus and method for error correction, according to the present invention, can be easily implemented with improved error-correction performance and be advantageous in cost.

[0043] Although a few preferred embodiments have been shown and described, it will be appreciated by those skilled in the art that various changes and modifications might be made without departing from the scope of the invention, as defined in the appended claims.

[0044] Attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

[0045] All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

[0046] Each feature disclosed in this specification (including any accompanying claims, abstract and drawings) may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

[0047] The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

Claims

1. An apparatus generating an error flag, the appara-

tus comprising:

a frame-sync error memory (130) which stores frame-sync error information for at least one data block;

a BIS Burst Indicator Subcode error flag memory (160) which stores a BIS error flag for the at least one data block; and

an error flag generator (150), which generates an error flag indicating an error existence/absence for ECC Error-Correction Coding data with reference to the frame-sync error information stored in the frame-sync error memory (130) and the BIS error flag stored in the BIS error flag memory (160).

2. The apparatus of claim 1, wherein the frame-sync error memory (130) stores frame-sync error information corresponding to at least two data blocks.

3. The apparatus of claim 1 or 2, wherein:

the at least one data block has an error correction format in which frame-sync data is recorded in a heading of the at least one data block and BIS data columns are recorded between sets of ECC data columns; and

the error flag generator (150) generates an error flag indicating an error existence for an entire ECC data constructing a set of ECC data columns with reference to error information stored in the frame-sync error memory (130) and the BIS error flag memory (160), if both the frame-sync error information of the frame-sync data and the BIS error flag of one of the BIS data columns neighboring a set of the ECC data columns, or the BIS error flag of the BIS data columns neighboring a pair of ECC data columns, indicate the error existence.

4. The apparatus of claim 1, 2 or 3, further comprising a frame-sync detector (110), which receives a reproduced digital signal for the at least one data block, determines the error existence/absence for frame-sync data for the at least one data block, and outputs frame-sync error information to the frame-sync error memory (130).

5. An error flag generation method comprising:

receiving a reproduced digital signal;

generating frame-sync error information for at least one data block using the reproduced digital signal;

storing the frame-sync error information in a frame-sync error memory (130) for the at least one data block;

generating a BIS error flag for the at least one data block;

storing the BIS error flag in a BIS error flag memory (160) for the at least one data block; and

generating an error flag indicating error existence/absence for ECC data with reference to the frame-sync error information stored in the frame-sync error memory (130) and the BIS error flag stored in the BIS error flag memory (160).

6. The method of claim 5, wherein the frame-sync error memory (130) stores frame-sync error information corresponding to at least two data blocks.

7. The method of claim 5 or 6, wherein the at least one data block has an error correction format in which frame-sync data is recorded in a heading of the at least one data block and BIS data columns are recorded respectively between sets of ECC data columns, and the generating of the error flag comprises generating an error flag indicating the error existence for entire ECC data constructing a set of ECC data columns, with reference to error information stored in the frame-sync error memory (130) and the BIS error flag memory (160), if both the frame-sync error information of the frame-sync data and the BIS error flag of a BIS data column neighboring the set of the ECC data columns, or the BIS error flag of the BIS data columns neighboring the set of the ECC data columns, indicate error existence.

8. An apparatus generating an error flag, comprising:

a frame-sync detector (110), outputting frame-sync error information indicating an existence/absence of an error for frame sync-data of frames forming data blocks;

a frame-sync error memory (130), storing the frame-sync error information of the frames forming the data blocks;

a BIS Burst Indicator Subcode error flag memory (160), storing a BIS error flag for the data blocks; and

an error flag generator (150), generating an error flag indicating an existence/absence of an error for ECC Error-Correction Coding data

with reference to the frame-sync error information stored in the frame-sync error memory (130) and the BIS error flag stored in the BIS error flag memory (160).

9. The apparatus of claim 8, wherein the frame-sync error memory (130) stores frame-sync error information corresponding to at least two data blocks.

10. The apparatus of claim 8 or 9, wherein the BIS error flag memory (160) stores BIS error flag corresponding to at least two data blocks.

11. The apparatus of claim 8, 9 or 10, wherein the frame-sync error memory (130) comprises a first through N-th frame-sync error memories.

12. The apparatus of claim 11, wherein N is at least two.

13. The apparatus of claim 11 or 12, wherein each of the frame-sync error memories has a size of 1x496 bits, and stores frame-sync error information of at least one data block.

14. The apparatus of any of claims 8 to 13, wherein the BIS error flag memory (160) comprises a first through an M-th BIS error memories.

15. The apparatus of claim 14, wherein M is at least two.

16. The apparatus of claim 14 or 15, wherein each of the BIS error memories has a size of 1x496 bits, and stores the BIS error flag of at least one data block.

17. The apparatus of any of claims 8 to 16, wherein each of the data blocks has an error correction format in which frame-sync data is recorded in a heading of the data block and BIS data columns are recorded between sets of ECC data columns.

18. The apparatus of claim 17, wherein the error flag generator (150), generates an error flag indicating the existence of an error for an entire ECC data forming a set of ECC data columns with reference to error information stored in the frame-sync error memory (130) and the BIS error flag memory (160), if the frame-sync error information of the frame-sync data and the BIS error flag of the BIS data column neighboring a set of the ECC data columns, or the BIS error flag of the BIS data columns neighboring a set of the ECC data columns, indicate error existence.

FIG. 1 (PRIOR ART)

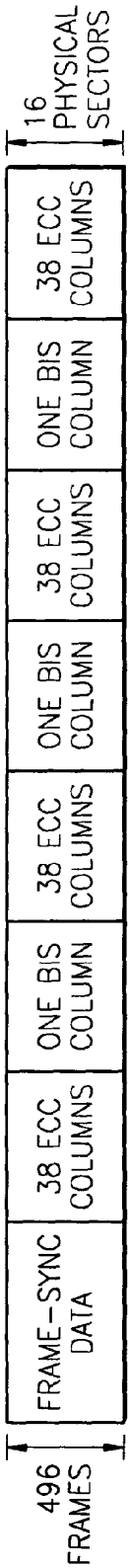


FIG. 2 (PRIOR ART)

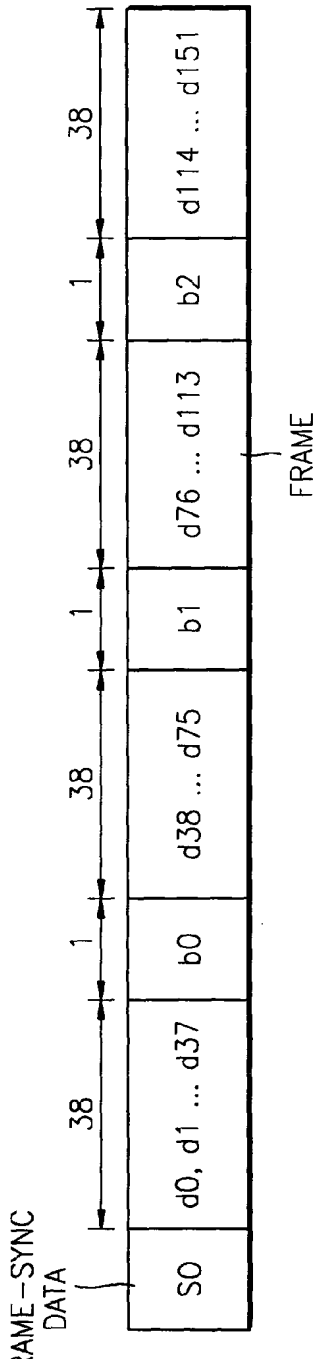
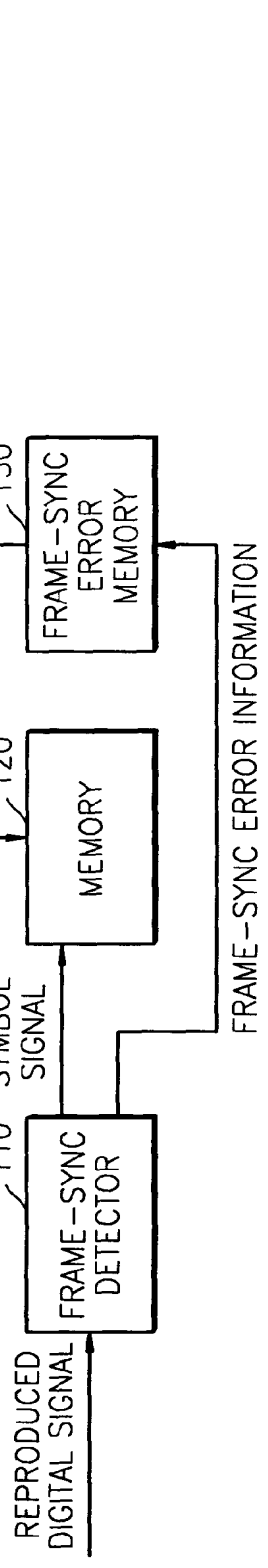


FIG. 3



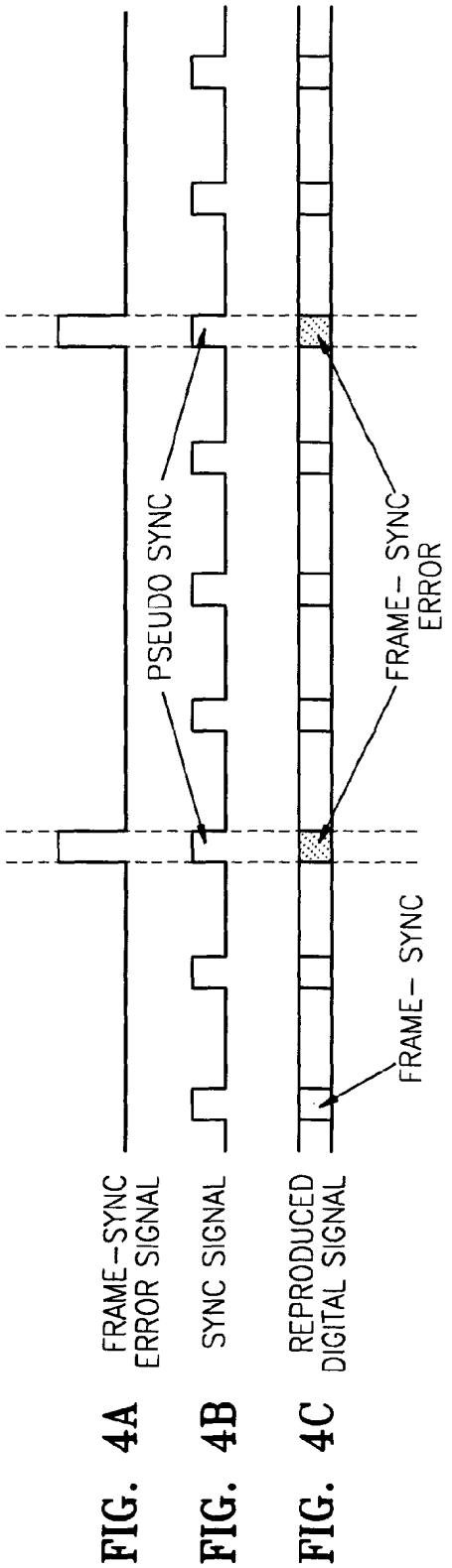


FIG. 4A

FIG. 4B

FIG. 4C

FIG. 5

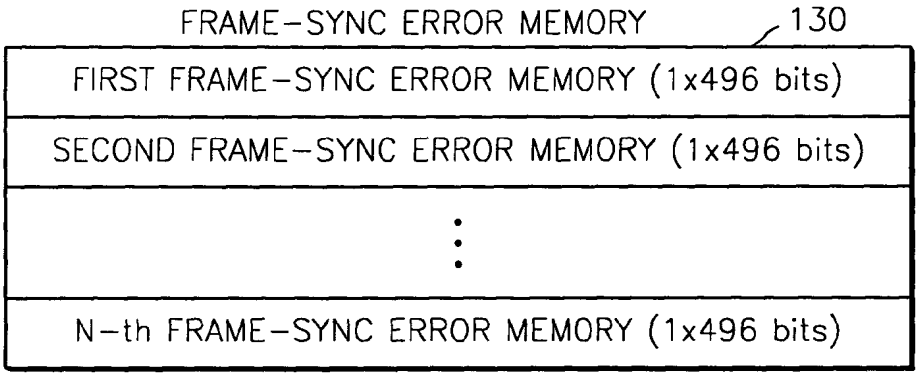

FRAME-SYNC ERROR MEMORY
130
FIRST FRAME-SYNC ERROR MEMORY (1x496 bits)
SECOND FRAME-SYNC ERROR MEMORY (1x496 bits)
N-th FRAME-SYNC ERROR MEMORY (1x496 bits)

FIG. 6

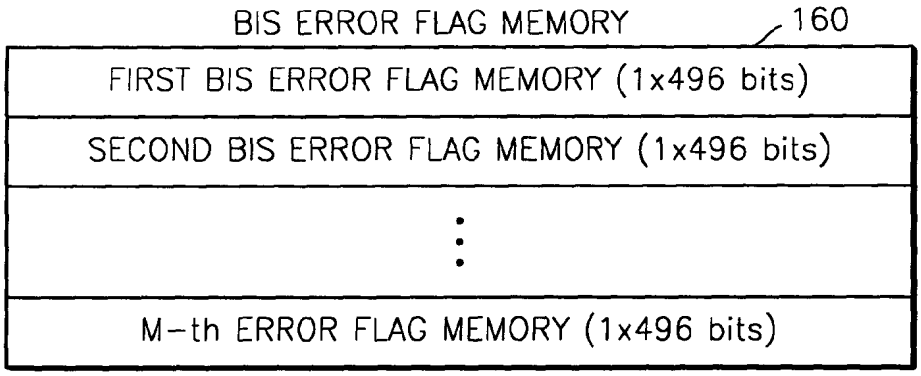
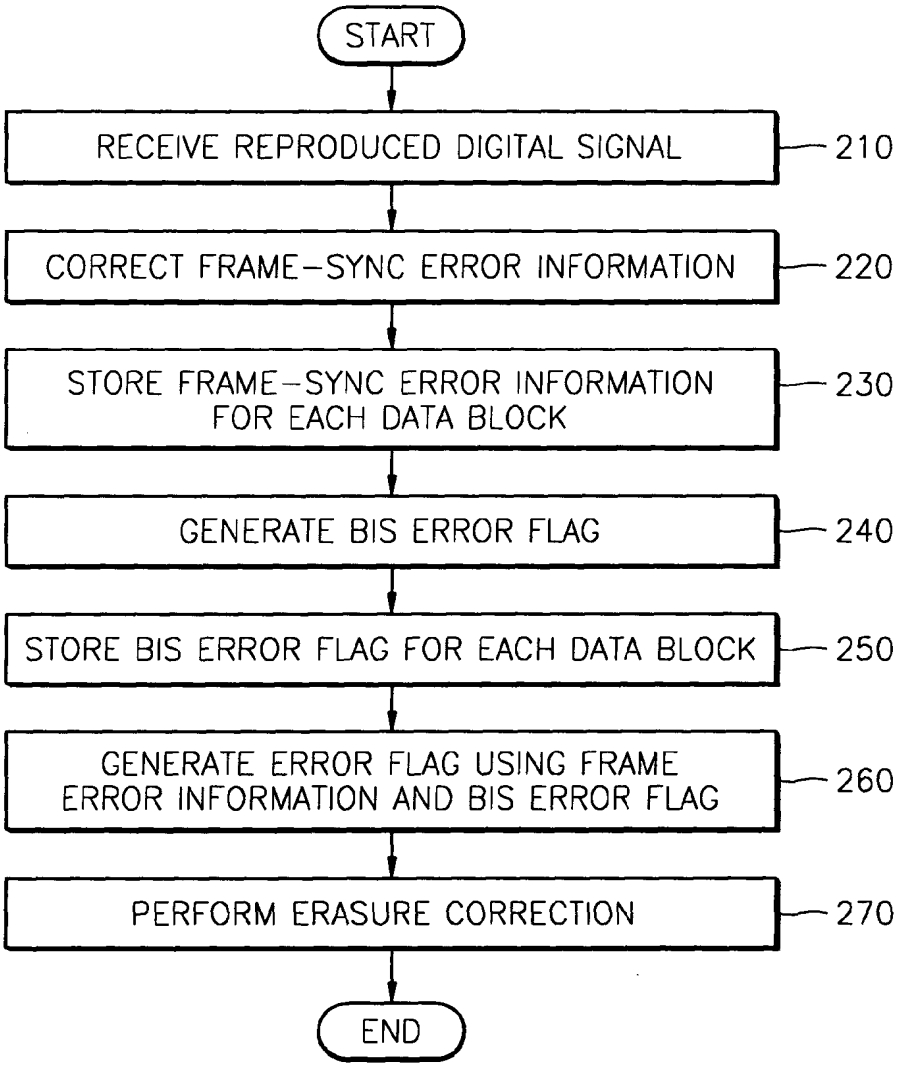

BIS ERROR FLAG MEMORY
160
FIRST BIS ERROR FLAG MEMORY (1x496 bits)
SECOND BIS ERROR FLAG MEMORY (1x496 bits)
M-th ERROR FLAG MEMORY (1x496 bits)

FIG. 7


START
RECEIVE REPRODUCED DIGITAL SIGNAL
210
CORRECT FRAME-SYNC ERROR INFORMATION
220
STORE FRAME-SYNC ERROR INFORMATION FOR EACH DATA BLOCK
230
GENERATE BIS ERROR FLAG
240
STORE BIS ERROR FLAG FOR EACH DATA BLOCK
250
GENERATE ERROR FLAG USING FRAME ERROR INFORMATION AND BIS ERROR FLAG
260
PERFORM ERASURE CORRECTION
270
END